ABSTRACT OF THE DISCLOSURE

An integrated memory can include a memory cell array, which has word lines for the selection of memory cells, bit lines for reading out or writing data signals of the memory cells, and a sense amplifier connected to bit lines of a bit line pair at one end of the bit line pair. In an activated state during a memory access, at least one activatable isolation circuit which is switched into one of the bit line pairs can isolate a part of the bit line pair, which is more remote from the sense amplifier from the sense amplifier. As a result, the effective capacitance of the bit lines can be significantly reduced during the memory access.